

In the Claims

This listing of claims will replace all prior versions, and listings, of claims.

Listing of Claims

1. (currently amended) A method of forming an integrated circuit transistor, comprising:

providing a semiconductor substrate with a gate structure formed thereon;

forming at least one dielectric layer overlying the semiconductor substrate, wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate;

forming at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer, wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region;

forming a sidewall spacer overlying the at least one dielectric layer along the at least one sidewall of the gate structure, wherein the sidewall spacer is formed using a blanket deposition process and a dry etch process; and

forming at least one second doped region in the semiconductor substrate laterally adjacent to the sidewall spacer.

2. (original) The method of forming an integrated circuit transistor of claim 1, wherein a thickness of the at least one dielectric layer ranges from about 10 Angstroms to about 350 Angstroms.

3. (original) The method of forming an integrated circuit transistor of claim 1, further comprising a step of removing exposed regions of the at least one dielectric layer before the formation of the at least one second doped region.

4. (original) The method of forming an integrated circuit transistor of claim 1, wherein the formation of the at least one dielectric layer is a blanket deposition of silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

5. (original) The method of forming an integrated circuit transistor of claim 1, wherein the formation of the at least one dielectric layer is a blanket deposition by a chemical vapor deposition (CVD) process using tetraethylorthosilicate (TEOS)

6. (original) The method of forming an integrated circuit transistor of claim 1, wherein the sidewall spacer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

7. (canceled)

8. (original) The method of forming an integrated circuit transistor of claim 1, wherein the at least one first doped region is formed using an ion implantation process and an annealing process

9. (original) The method of forming an integrated circuit transistor of claim 8, wherein after the annealing process, the at least one dielectric layer becomes a densified material which exhibits an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

10-15. (canceled)

16-22. (canceled)